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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,906	10/31/2003	Robert O. Conn	X-1416-2 US	3002

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EXAMINER	
TRAN, THANH Y	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 06/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/698,906	CONN, ROBERT O.	
	Examiner	Art Unit	
	Thanh Y. Tran	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6-18 and 20* is/are rejected.

7)☒ Claim(s) *2-5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/16/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 9 and 17 recite the limitation "the caposer" in line 2 (claim 9), and in line 1 (claim 17). There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 6-10, 12-18 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamagishi et al (U.S. 2004/0239349).

As to claim 1, Yamagishi et al discloses in figure 4 an assembly comprising: a printed circuit board ("probe card" 10) comprising a conductor (a conductor is a dark layer in board 10), the conductor having a characteristic impedance [*see paragraph [0043], probe card 10 has an impedance, thus conductor of probe card 10 having a characteristic impedance*], an integrated circuit die (chip 30) having an output driver, the output driver having an output impedance [see paragraph [0042], semiconductor chip 30 having an impedance, thus it has an output impedance], an integrated circuit package ("core layer" 12) having an inside surface; and an interposer ("interconnection layer" 14) disposed in the integrated circuit package between the integrated circuit (30) and the inside surface of the integrated circuit package (12), wherein a signal path extends from

the output driver (output of chip 30), through the interposer (14), through the package (12), and to the conductor of the printed circuit board (10), the signal path (signal path is the path/trace that connects the output of chip 30 to the conductor of board 10) exhibiting an intervening impedance, wherein the output impedance of the output driver (output of chip 30) plus the intervening impedance of the signal path substantially equals the characteristic impedance of the conductor of the printed circuit board (10) [*see paragraphs [0042] and [0043], the output impedance of semiconductor chip 30 and the impedance of the signal path (impedance of the signal path having a capacitor) is substantially equal to the impedance of the conductor of the printed circuit board (probe card 10)*].

As to claim 6, Yamagishi et al discloses in figure 4 an assembly, wherein the integrated circuit (chip 30) includes a micro-bump (32), and wherein the output driver (output of chip 30) is coupled through the micro-bump (32) to the interposer (14).

As to claim 7, Yamagishi et al discloses in figure 4 an assembly, wherein the interposer (14) is a through-hole interposer (see the vias/holes in the interposer 14).

As to claim 8, Yamagishi et al discloses in figure 4 an assembly, wherein the interposer (14) is a via interposer (see the vias/holes in the interposer 14).

As to claim 9, Yamagishi et al discloses in figure 4 an assembly, wherein the integrated circuit die (chip 30) has a major surface, and wherein the interposer (14) has a major surface, the major surface of the integrated circuit die (30) and the major surface of the interposer (14) having roughly identical surface areas.

As to claim 10, Yamagishi et al discloses in figure 4 an assembly, wherein the interposer (14) includes no transistor and no PN junction.

As to claim 12, Yamagishi et al discloses in figure 4 an assembly, wherein the interposer includes a layer of resistive material ("thin film resistor") (see paragraph [0004]), wherein a portion of the layer of resistive material is a resistor ("thin film resistor"), the resistor inherently having a resistance, and wherein the impedance of the intervening impedance (impedance of the signal path/trace) depends at least in part on the resistance of the resistor ("thin film resistor").

As to claim 13, Yamagishi et al discloses in figure 4 an assembly, wherein the interposer includes a first conductive layer (see the first dark trace/conductor in the interposer 14) and a second conductive layer (see the second dark trace/conductor in the interposer 14), the first and second conductive layers constituting a capacitor (20), the capacitor (20) having a capacitance, and wherein the impedance of the intervening impedance (impedance of the signal path/trace) depends at least in part on the capacitance of the capacitor (20).

As to claim 14, Yamagishi et al discloses in figure 4 an assembly, wherein the interposer (14) comprises a micro-bump ("Cu plugs") (as indicated at 14-2c in figure 7c), the interposer (14) being coupled to the inside surface of the integrated circuit package (12) by the micro-bump (14-2c).

As to claim 15, Yamagishi et al discloses in figure 4 an assembly and a corresponding method of impedance matching an output driver of an integrated circuit die (chip 30) to a printed circuit board conductor (see dark traces/layer in probe card 10), the output driver exhibiting an output impedance (output of chip 30 having an output impedance), the printed circuit board conductor exhibiting a characteristic impedance, the method comprising: providing an interposer (14) in a signal path/trace, wherein the signal

path (signal trace) extends from the output driver (output of chip 30) and to the printed circuit board conductor (conductor is a dark trace/layer in probe card 10), wherein the signal path (signal trace) from the output driver (output of chip 30) to the printed circuit board conductor (conductor/trace of 10) exhibits an intervening impedance (see paragraphs [0042] and [0043]), wherein the output impedance (output impedance of chip 30) plus the intervening impedance (impedance of signal path) is substantially equal to the characteristic impedance (impedance of the printed circuit board conductor), the interposer (14) being disposed inside an integrated circuit package between the integrated circuit die (30) and an inside surface of the integrated circuit package (12). [*see paragraphs [0042] and [0043], the output impedance of semiconductor chip 30 and the impedance of the signal path (impedance of the signal path having a capacitor) is substantially equal to the impedance of the conductor of the printed circuit board (probe card 10)*].

As to claim 16, Yamagishi et al discloses in figure 4 an assembly and a corresponding method, wherein the integrated circuit die (chip 30) has a micro-bump (32), the integrated circuit die (30) being physically attached to the interposer (14) by the micro-bump (32) of the integrated circuit die (30), and wherein the interposer (14) has a micro-bump ("Cu plugs") (as indicated at 14-2c in figure 7c), the interposer (14) being physically attached to the integrated circuit package (12) by the micro-bump of the interposer (14).

As to claim 17, Yamagishi et al discloses in figure 4 an assembly and a corresponding method, wherein the interposer has a planar form and is less than 100 microns thick ("thickness of 45 .mu.m.") (see paragraph [0099]).

As to claim 18, Yamagishi et al discloses in figure 4 an assembly comprising: an integrated circuit die (chip 30) having a micro-bump (32) and an output driver (output of chip 30), the output driver exhibiting an output impedance (see paragraph [0042]); an integrated circuit package containing the integrated circuit die (chip 30); a conductor (comprising "probe" 16 and conductive pads on card 10) disposed outside the integrated circuit package, the conductor exhibiting a characteristic impedance; means (14) for inserting an impedance into a signal path between the output driver (output of chip 30) and the conductor (conductor of card 10) (see paragraphs [0042] and [0043]), the means (14) being physically attached to the integrated circuit die (30) by the micro-bump (32) of the integrated circuit die (30), the means (14) including a micro-bump ("Cu plugs") (as indicated at 14-2c in figure 7c) that physically attaches the means (14) to the integrated circuit package (12); and wherein the signal path (signal trace) between the output driver (output of chip 30) and the conductor (conductor of 10) exhibits an intervening impedance, and wherein the intervening impedance (impedance of signal path) plus the output impedance (output impedance of semiconductor chip 30) is substantially equal to the characteristic impedance (impedance of the conductor of the printed circuit board 10) [*see paragraphs [0042] and [0043], the output impedance of semiconductor chip 30 and the impedance of the signal path (impedance of the signal path having a capacitor) is substantially equal to the impedance of the conductor of the printed circuit board (probe card 10)*].

As to claim 20, Yamagishi et al discloses in figure 4 an assembly, wherein the means (14) includes no transistor and no PN junction.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamagishi et al (U.S. 2004/0239349).

As to claim 11, Yamagishi et al does not disclose the interposer includes a layer comprising epoxy and fiberglass. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the assembly of Yamagishi et al by using epoxy and fiberglass materials for a layer of the interposer for improving the reliability of the interposer/interconnection for the package and reducing production cost, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended used as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Allowable Subject Matter

6. Claims 2-5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zandra V. Smith
Supervisory Patent Examiner
12 June 2006

TYT